Patent Search

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Abstract:

The invention discloses a hybrid-pipelined Fast Fourier Transform (FFT) architecture optimized for high-speed and resource-efficient FPGA implementation. The system int selective parallel Processing Units with stage-wise pipelined butterfly blocks, enabling continuous real-time computation of 16-point FFTs with reduced latency and improv throughput. A twiddle-factor multiplication module employing reduced-precision arithmetic minimizes DSP usage, while FIFO-based delay and alignment structures ensure correct sequencing across pipeline stages. A deterministic control and synchronization unit governs data flow, stage timing, and parallel-lane routing, eliminating stalls and conditions. The architecture supports scalable configurations, reduced power consumption, and simplified routing, offering significant performance and economic advanta communication systems, radar processing, biomedical analytics, and other real-time digital signal-processing applications.

Complete Specification

Description:FIELD OF THE INVENTION

[001] The present invention relates to the field of digital signal processing (DSP), VLSI/FPGA-based hardware architectures, and high-performance computational systems More particularly, the invention pertains to the design and implementation of an optimized Hybrid-Pipelined Fast Fourier Transform (FFT) architecture suitable for low-power, low-latency, and high-throughput signal-processing applications. The invention further relates to FFT structures that selectively integrate parallel processing stage pipelined computation units, twiddle-factor multiplier optimization, and FIFO-based memory organization to achieve improved performance on FPGA platforms for wirel communication, biomedical signal processing, and real-time spectral-analysis systems.

BACKGROUND OF THE INVENTION

[002] Fast Fourier Transform (FFT) computation forms the computational backbone of numerous signal-processing applications, including wireless communication, OFDM modulation, radar and sonar processing, biomedical analytics, audio spectrum analysis, and high-speed instrumentation. Conventional FFT architectures implemented o FPGA platforms generally adopt one of three classical design paradigms: radices-2/4 iterative architectures, fully parallel architectures, or pipelined streaming architectur such as Single-Path Delay Feedback (SDF) and Multi-Path Delay Commutator (MDC) structures. While these prior-art approaches are widely used, each suffers from inher architectural inefficiencies that limit throughput, flexibility, or hardware efficiency when deployed in modern, high-performance FPGA systems

View Application Status