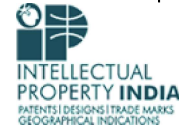


Home (<https://ipindia.gov.in/>) About Us (<https://ipindia.gov.in/Home/AboutUs>) Policy & Programs (<https://ipindia.gov.in/Home/policypages>)
 Achievements (<https://ipindia.gov.in/Home/achievementspage>) RTI (<https://ipindia.gov.in/Home/righttoinformation>)
 Sitemap (<https://ipindia.gov.in/Home/Sitemap>) Contact Us (<https://ipindia.gov.in/Home/contactus>)

[Skip to Main Content](#)



(<http://ipindia.nic.in/index.htm>)



(<http://ipindia.nic.in/ind>)

Patent Search

Invention Title	Hybrid-Pipelined Parallel FFT Architecture for High-Speed FPGA Processing
Publication Number	01/2026
Publication Date	02/01/2026
Publication Type	INA
Application Number	202541126299
Application Filing Date	13/12/2025
Priority Number	
Priority Country	
Priority Date	
Field Of Invention	COMPUTER SCIENCE
Classification (IPC)	G06F 17/14, G06F 9/38, G06F 9/30, G06F 7/544, G06F 7/523

Inventor

Name	Address	Country	Nat
Dr. G Prasanna Kumar	Professor, Department of ECE, Vishnu Institute of Technology, Vishnupur, Bhimavaram, West Godavari District, Andhra Pradesh 534202	India	Indi
Dr. B V V Satyanarayana	Professor, Department of ECE, Vishnu Institute of Technology, Vishnupur, Bhimavaram, West Godavari District, Andhra Pradesh 534202	India	Indi
D Durga Prasad	Assistant Professor, Department of ECE, Vishnu Institute of Technology, Vishnupur, Bhimavaram, West Godavari District, Andhra Pradesh 534202	India	Indi
A K Chaitanya Varma	Associate Professor, Department of ECE, Vishnu Institute of Technology, Vishnupur, Bhimavaram, West Godavari District, Andhra Pradesh 534202	India	Indi
M Dileep	Associate Professor, Department of ECE, Vishnu Institute of Technology, Vishnupur, Bhimavaram, West Godavari District, Andhra Pradesh 534202	India	Indi
M V Pathi Amudalapalli	Assistant Professor, Department of ECE, Vishnu Institute of Technology, Vishnupur, Bhimavaram, West Godavari District, Andhra Pradesh 534202	India	Indi
Prudhvi Raj Budumuru	Assistant Professor, Department of ECE, Vishnu Institute of Technology, Vishnupur, Bhimavaram, West Godavari District, Andhra Pradesh 534202	India	Indi

Applicant

Name	Address	Country	Nation
Vishnu Institute of Technology	Sri Vishnu Education Society, Kowada Rd, Vishnupur, Kowada, Andhra Pradesh 534202	India	India

Abstract:

The invention discloses a hybrid-pipelined Fast Fourier Transform (FFT) architecture optimized for high-speed and resource-efficient FPGA implementation. The system integrates selective parallel Processing Units with stage-wise pipelined butterfly blocks, enabling continuous real-time computation of 16-point FFTs with reduced latency and improved throughput. A twiddle-factor multiplication module employing reduced-precision arithmetic minimizes DSP usage, while FIFO-based delay and alignment structures ensure correct sequencing across pipeline stages. A deterministic control and synchronization unit governs data flow, stage timing, and parallel-lane routing, eliminating stalls and conditions. The architecture supports scalable configurations, reduced power consumption, and simplified routing, offering significant performance and economic advantages for communication systems, radar processing, biomedical analytics, and other real-time digital signal-processing applications.

Complete Specification**Description: FIELD OF THE INVENTION**

[001] The present invention relates to the field of digital signal processing (DSP), VLSI/FPGA-based hardware architectures, and high-performance computational systems. More particularly, the invention pertains to the design and implementation of an optimized Hybrid-Pipelined Fast Fourier Transform (FFT) architecture suitable for low-power, low-latency, and high-throughput signal-processing applications. The invention further relates to FFT structures that selectively integrate parallel processing stage pipelined computation units, twiddle-factor multiplier optimization, and FIFO-based memory organization to achieve improved performance on FPGA platforms for wireless communication, biomedical signal processing, and real-time spectral-analysis systems.

BACKGROUND OF THE INVENTION

[002] Fast Fourier Transform (FFT) computation forms the computational backbone of numerous signal-processing applications, including wireless communication, OFDM modulation, radar and sonar processing, biomedical analytics, audio spectrum analysis, and high-speed instrumentation. Conventional FFT architectures implemented on FPGA platforms generally adopt one of three classical design paradigms: radixes-2/4 iterative architectures, fully parallel architectures, or pipelined streaming architectures such as Single-Path Delay Feedback (SDF) and Multi-Path Delay Commutator (MDC) structures. While these prior-art approaches are widely used, each suffers from inherent architectural inefficiencies that limit throughput, flexibility, or hardware efficiency when deployed in modern, high-performance FPGA systems.

[View Application Status](#)


Terms & conditions (<https://ipindia.gov.in/Home/Termsconditions>) Privacy Policy (<https://ipindia.gov.in/Home/Privacypolicy>)

Copyright (<https://ipindia.gov.in/Home/copyright>) Hyperlinking Policy (<https://ipindia.gov.in/Home/hyperlinkingpolicy>)

Accessibility (<https://ipindia.gov.in/Home/accessibility>) Contact Us (<https://ipindia.gov.in/Home/contactus>) Help (<https://ipindia.gov.in/Home/help>)

Content Owned, updated and maintained by Intellectual Property India, All Rights Reserved.

Page last updated on: 26/06/2019