## Patent Search

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**Abstract:**

The invention provides a multiplier-free finite impulse response (FIR) filter architecture employing an Array Product Generator (APG) and a multiplexer-based partial produ selector (APM) to perform convolution without hardware multipliers. An input shift-register array supplies bitwise sample values to the APG, which generates coefficient-dependent partial products using precomputed bit patterns stored in coefficient memory. A multiplexer network selects the appropriate partial products, which are routec through an alignment network and accumulated in a pipelined adder structure to produce the final FIR output. A centralized control and timing unit synchronizes all computational stages, while an output register provides stable filtered results. The architecture achieves reduced hardware complexity, lower power consumption, and hig throughput performance suitable for FPGA and VLSI platforms.

Complete Specification

Description:FIELD OF THE INVENTION

[001] The present invention relates generally to the field of digital signal processing (DSP) and hardware-efficient implementation of finite impulse response (FIR) filters o integrated circuits. More particularly, the invention pertains to a multiplier-free FIR filter architecture suitable for Very-Large-Scale Integration (VLSI) and Field-Programma Gate Array (FPGA) platforms, wherein filter products are generated without the use of conventional hardware multipliers. The invention utilizes an Array Product Generat (APG) and a Multiplexer-based selection mechanism (APM/MUX) configured to replace multiplier operations with shift-and-add logic and coefficient-decoded patterns, thereby achieving significantly reduced hardware complexity, lower power consumption, improved area–delay performance, and enhanced suitability for low-power and high-speed DSP applications.

BACKGROUND OF THE INVENTION

[002] Finite Impulse Response (FIR) filters constitute a fundamental building block in a wide range of digital signal-processing (DSP) applications, including wireless communication systems, biomedical instrumentation, audio and speech processing, radar systems, and embedded sensor processing. Traditional FIR filter implementati rely on the multiply–accumulate (MAC) paradigm, wherein each filter tap requires a multiplication between an input sample and its corresponding coefficient followed by accumulation operation. As filter orders increase or high-throughput operation is required, the number of multipliers grows proportionally, thereby imposing substantial

View Application Status