(12) PATENT APPLICATION PUBLICATION

(21) Application No.202041044774 A

(19) INDIA

(22) Date of filing of Application :14/10/2020

(43) Publication Date : 23/10/2020

		and a charling of the
	le le	(71)Name of Applicant :1)Dr Vikram Palodiya, Sreenidhi Institute of science and
		Teshaology
		Address of Applicant : Assistant professor, ECE Sreenidhi Institute of science and Technology Yanampet Hyderabad Telangana India 501301
	. 1	Telengana India
	a far i na	2)Dr Syed Jahangir Badashah, Sreenidhi Institute of science and
		Technology 3)Dr Shaik Shafiulla Basha,Y.S.R. Engineering college of Yogi
		Vemana University
	1. AP	 4)Dr.Prakash Pareek, Vishnu Institute of Technology (Autonomous) 5)Dr B P Santosh Kumar, Y.S.R. Engineering college of Yogi
		Vemana University 6)Dr. Sushma Jaiswal,CSIT,Guru Ghasidas Central University 7)Dr. Vipin Kumar Garg,Meerut Institute of Engineering &
in the section	:A61B	Technology
51) International classification	5/00	8)Kalyan Singh,Guru Jambheshwar University of Science and
 Priority Document No Priority Date 	:NA :NA	Technology 9)Krishan Kumar,Guru Jambheshwar University of Science and
33) Name of priority country86) International Application No	:NA :NA	Technology 10)Dr. Dhirendra Kumar Shukla, Regional Institute of Education,
Filing Date	:NA	NCERT
(87) International Publication No	: NA :NA	(72)Name of Inventor :
(61) Patent of Addition to Application Number	:NA	1)Dr Vikram Palodiya, Sreenidhi Institute of science and
Filing Date (62) Divisional to Application Number	:NA :NA	Technology 2)Dr Syed Jahangir Badashah,Sreenidhi Institute of science and
Filing Date		Technology 3)Dr Shaik Shafiulla Basha,Y.S.R. Engineering college of Yogi
		Vemana University 4)Dr.Prakash Pareek, Vishnu Institute of Technology (Autonomou 5)Dr B P Santosh Kumar, Y.S.R. Engineering college of Yogi
		Vemana University
		6)Dr. Sushma Jaiswal,CSIT,Guru Ghasidas Central University 7)Dr. Vipin Kumar Garg,Meerut Institute of Engineering &
		Technology
		8)Kalyan Singh,Guru Jambheshwar University of Science and
		Technology 9)Krishan Kumar,Guru Jambheshwar University of Science and
		Technology
		10)Dr. Dhirendra Kumar Shukla, Regional Institute of Education

(57) Abstract :

In the current pandemic situation, patients with critical diseases are lacking immediate care which would reduce the mortality rate. This invention focuses on continuous monitoring of patientâtms EEG signals for occurrence of any seizures in brain signals. This system is designed using machine learning algorithm for resource optimization thereby implemented using VLSI technology. The proposed algorithm provides competitive performance as it requires EEG signals only from front and frontal temporal lobes instead of signals from standard full EEG system. Seizure detection is accurate just by easily mountable headsets of dry electrode without the need of painful through- hair electrodes which is highly uncomfortable and uses adhesive material. Compact VLSI implementation is uploaded on low power FPGA Actel Igloo AGL250 that consumes 110 Watts of dynamic power and required 1237 logical elements, operating at a detection latency of 10.2 seconds provides specificity of 80.2% and sensitivity of detection as 92.6%.

No. of Pages : 13 No. of Claims : 6

The Patent Office Journal No. 43/2020 Dated 23/10/2020

54449

 Home (http://ipindia.nic.in/index.htm)
 About Us (http://ipindia.nic.in/about-us.htm)
 Who's Who (http://ipindia.nic.in/whos-who-page.htm)

 Policy & Programs (http://ipindia.nic.in/policy-pages.htm)
 Achievements (http://ipindia.nic.in/achievements-page.htm)

 RTI (http://ipindia.nic.in/right-to-information.htm)
 Feedback (https://ipindiaonline.gov.in/feedback)
 Sitemap (shttp://ipindia.nic.in/itemap.htm)

Contact Us (http://ipindia.nic.in/contact-us.htm) Help Line (http://ipindia.nic.in/helpline-page.htm)

Skip to Main Content Screen Reader Access (screen-reader-access.htm)

CALL ADVANCED SEARCH System



INTELLECTUAL PROPERTY INDIA Atents Idesigns I Trade Marks Geogramicu Indications

(http://ipindia.nic.in/inc

Patent Search

Invention Title	VLSI BASED	EEG SIGNAL PROCESSING FOR SMART PATIENT MONITORING SYSTEM				
Publication Number	43/2020					
Publication Date	23/10/2020					
Publication Type	INA					
Application Number	202041044774					
Application Filing Date	14/10/2020					
Priority Number						
Priority Country						
Priority Date						
Field Of Invention	MECHANICAL ENGINEERING					
Classification (IPC)	A61B 5/00					
Inventor						
Name		Address	Country	Nat		
Dr Vikram Palodiya, Sreenidhi Institute of science and Technology		Assistant professor, ECE Sreenidhi Institute of science and Technology Yanampet Hyderabad Telangana India 501301	India	Ind		
Dr Syed Jahangir Badashah,Sreenidhi Institute of science and Technology		Professor, ECE, Sreenidhi Institute of science and Technology Yanampet Hyderabad Telangana India 501301	India	Ind		
Dr Shaik Shafiulla Basha,Y.S.R. Engineering college of Yogi Vemana University		Assistant Professor, ECE,Y.S.R. Engineering college of Yogi Vemana University YMR Colony, Korrapadu Road Proddatur, Andhra Pradesh India 516360	India	Ind		
Dr.Prakash Pareek,Vishnu Institute of Technology (Autonomous)		Associate Professor, ECE, Vishnu Institute of Technology (Autonomous) Vishnupur, Kovvada Rd, Kovvada Bhimavaram Andhra Pradesh India 534202	India	Ind		
Dr B P Santosh Kumar,Y.S.R. Engineering college of Yogi Vemana University		Assistant Professor, ECE, Y.S.R. Engineering college of Yogi Vemana University YMR Colony, Korrapadu Road Proddatur, Andhra Pradesh India 516360		Ind		
Dr. Sushma Jaiswal,CSIT,Guru Central University	ı Ghasidas	Assistant Professor, CSIT,Guru Ghasidas Central University C.G, Koni, Bilaspur Chhattisgarh India 495009	India	Ind		
Dr. Vipin Kumar Garg,Meerut Engineering & Technology	Institute of	Professor&Head, Department of Pharmaceutical Technology, Meerut Institute of Engineering & Technology NH-58, Baghpat Bypass crossing Road, Delhi Haridwar Highway Meerut Uttar Pradesh India 250005	India	Ind		
Kalyan Singh,Guru Jambheshwar University of Science and Technology		Assistant Professor, Dept of Electrical Engineering, Guru Jambheshwar University of Science and Technology Hisar Hisar Haryana India 125001	India	Ind		
Krishan Kumar,Guru Jambheshwar University of Science and Technology		Assistant Professor, Dept of Electrical Engineering, Guru Jambheshwar University of Science and Technology	India	Ind		
· ·		Hisar Hisar Haryana India 125001				

Name	Address		Nat
Dr Vikram Palodiya, Sreenidhi Institute of science and Technology	Assistant professor, ECE Sreenidhi Institute of science and Technology Yanampet Hyderabad Telangana India 501301		Indi
Dr Syed Jahangir Badashah,Sreenidhi Institute of science and Technology	Professor, ECE, Sreenidhi Institute of science and Technology Yanampet Hyderabad Telangana India 501301		Indi
Dr Shaik Shafiulla Basha,Y.S.R. Engineering college of Yogi Vemana University	Assistant Professor, ECE,Y.S.R. Engineering college of Yogi Vemana University YMR Colony, Korrapadu Road Proddatur, Andhra Pradesh India 516360		Indi
Dr.Prakash Pareek,Vishnu Institute of Technology (Autonomous)	Associate Professor, ECE, Vishnu Institute of Technology (Autonomous) Vishnupur, Kovvada Rd, Kovvada Bhimavaram Andhra Pradesh India 534202		Indi
Dr B P Santosh Kumar,Y.S.R. Engineering college of Yogi Vemana University	Assistant Professor, ECE, Y.S.R. Engineering college of Yogi Vemana University YMR Colony, Korrapadu Road Proddatur, Andhra Pradesh India 516360		Indi
r. Sushma Jaiswal,CSIT,Guru Ghasidas Assistant Professor, CSIT,Guru Ghasidas Central University C.G, Koni, Bilaspur Chhattisgarh India 495009 entral University		India	Indi
Dr. Vipin Kumar Garg, Meerut Institute of Professor & Head, Department of Pharmaceutical Technology, Meerut Institute of Engineering & Technology NH-58, Baghpat Bypass crossing Road, Delhi Haridwar Highway Meerut Uttar Pradesh India 250005		India	Indi
Kalyan Singh,Guru Jambheshwar University of Science and Technology			Indi
Krishan Kumar,Guru Jambheshwar University of Science and Technology	Assistant Professor, Dept of Electrical Engineering, Guru Jambheshwar University of Science and Technology Hisar Hisar Haryana India 125001		Indi
Dr. Dhirendra Kumar Shukla,Regional Institute of Education, NCERT	Regional Institute of Education, NCERT Jahanuma Palace, Shaymla Hills Bhopal Madhya Pradesh India 462013	India	Indi

Abstract:

In the current pandemic situation, patients with critical diseases are lacking immediate care which would reduce the mortality rate. This invention focuses on continuous monitoring of patient's EEG signals for occurrence of any seizures in brain signals. This system is designed using machine learning algorithm for resource optimization the implemented using VLSI technology. The proposed algorithm provides competitive performance as it requires EEG signals only from front and frontal temporal lobes inste signals from standard full EEG system. Seizure detection is accurate just by easily mountable headsets of dry electrode without the need of painful through- hair electrode is highly uncomfortable and uses adhesive material. Compact VLSI implementation is uploaded on low power FPGA Actel Igloo AGL250 that consumes 110 Watts of dynam power and required 1237 logical elements, operating at a detection latency of 10.2 seconds provides specificity of 80.2% and sensitivity of detection as 92.6%.

Complete Specification

Claims:1. EEG based seizure detection is done by resource optimized VLSI architecture for smart patient monitoring.

2. EEG signal collection is painless as dry electrode EEG headset is used for frontal and front temporal lobe EEG signals.

3. Dry electrodes are quickly mountable providing reliable EEG signals even from head part covered with hair with low signal quality.

4. Machine algorithm is developed for EEG signal analysis for detection of any epilepsy seizures in EEG signals.

5. Actel Igloo AGL250 low power FPGA is utilized for implementing the algorithm with power consumption of 110 watts and latency of 10 seconds.

6. Sensitivity of seizure detection is about 93% and specificity of about 80%. , Description:? In this invention different sets of FIR coefficients specific for channel are retrie with a constant range of input address of Flash ROM with 0-30 channel specific address offset can be added selectively to each of the input address by using offset multiplexer for facilitating retrieval of coefficient in shared structure of FIR.

? Same concept can be used for storage of FIR input data and retrieval inside RAM of the system.

? Signals from FIR filter has to be processed using 8 channels only which involves 32 input data from each of the channel which has to the stored and accessed in an efficient way in one of the RAM block on FPGA.

? Data storage and retrieval for different sets of channel specific input data of FIR filter involves only constant value of RAM input address of 0-30 values which is specific each channel RAM offset address.

? As a result, with minimal additional LE cost, this address offset methods easily converts a single channel FIR to a configurable multichannel FIR filter using multiplexers. ? The resource-optimized VI SI implementation was uploaded onto a low-power Microsemi FPGA (AGI 250)

View Application Status



Terms & conditions (http://ipindia.gov.in/terms-conditions.htm) Privacy Policy (http://ipindia.gov.in/privacy-policy.htm)

Copyright (http://ipindia.gov.in/copyright.htm) Hyperlinking Policy (http://ipindia.gov.in/hyperlinking-policy.htm)

Accessibility (http://ipindia.gov.in/accessibility.htm) Archive (http://ipindia.gov.in/archive.htm) Contact Us (http://ipindia.gov.in/contact-us.htm) Help (http://ipindia.gov.in/help.htm)

Content Owned, updated and maintained by Intellectual Property India, All Rights Reserved.

Page last updated on: 26/06/2019